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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,139	01/22/2004	Cheng-Hsun Tsai	3304.2.118	6399

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,139	TSAI, CHENG-HSUN	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-10, 12-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (U.S Pub. 2003/0079909) in view of King et al. (U.S Pat. 5,677,566).

Regarding claims 1, 9 and 15, Nguyen (Fig. 2) discloses a stacked IC comprising: a first IC package unit $110_{(K+1)}$ comprising an IC chip (paragraph [0014]), an encapsulant resin (paragraph [0014], lines 13-14 and lines 19-24), and a plurality of lead wires 272/274 comprises a first end encapsulated by the encapsulant resin and a second end extending outside the encapsulant resin, wherein the second end extending outside the encapsulant resin comprises first and second soldering portions (see Fig. 2); a second IC package unit $110_{(K)}$ having the same structure as the first IC package unit $110_{(K+1)}$ (paragraph [0014], lines 19-24); and an interface layer 210 sandwiched between the first IC package unit $110_{(K+1)}$ and the second IC package unit $110_{(K)}$, and having first and second sides with a plurality of soldering pads 222/224 and 232/234, wherein each first soldering portion of the first IC package unit $110_{(K+1)}$ is connected to corresponding soldering pad 232/234 on the first side of the interface layer 210 via a

solder bump 262/264, and each second soldering portion of the second IC package unit $110_{(K)}$ is connected to corresponding soldering pad 222/224 on the second side of the interface layer 210 via a soldering material other than the solder ball (not labeled, see Fig. 2), thereby achieving electrical connection between the first IC package unit $110_{(K+1)}$ and the second IC package unit $110_{(K)}$ (paragraph [0020], lines 1-5). Nguyen (Fig. 2) further discloses that the first and second IC units $110_{(K+1)}$ and $110_{(K)}$ are selected from TSOP (paragraph [0014], lines 19-24). It is noted that one skilled in the art would recognize that the first end of the lead wire 272/274 would be electrically connected to the IC chip encapsulated in the encpasulant resin in order to transfer the data signals to and from the IC chip, as taught by Fig. 8 of King.

Nguyen does not disclose that the solder bump 262/264 formed on the first soldering portion of the lead wire 272/274 is a solder ball.

However, King (Fig.8) teaches the forming of an IC package unit having the lead wires 12, each comprise a first end 13 connected to an IC chip 14 and a second end 15 extending outside the encapsulant resin 26 (column 4, lines 35-37), wherein each lead wire 12 has a solder ball 28 (column 4, lines 49-50) positioned at "desired locations along conductive lead wire 12" (column 3, lines 32-33). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use a solder ball for the solder bump 262/264 formed on the first soldering portion of the lead wire 272/274 of Nguyen because the solder ball is commonly used for serving as the external electrode for surface mounting on a printed circuit board, as taught by King (column 4, lines 56-65).

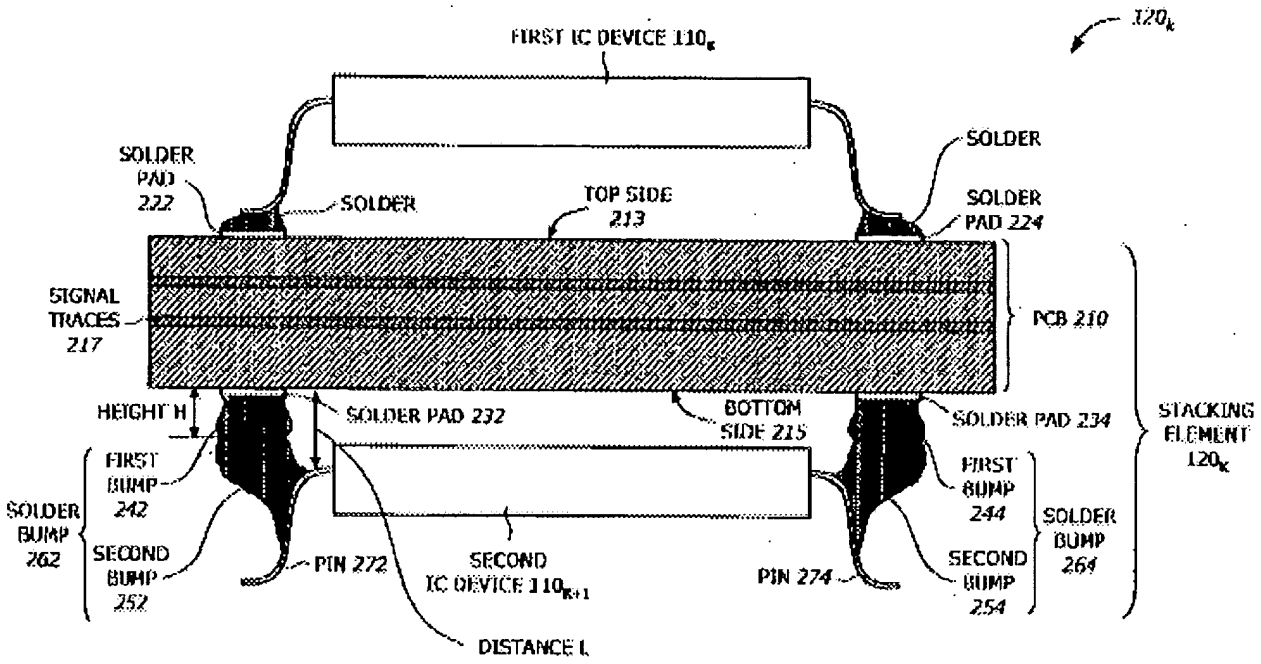

FIG. 2

Regarding claim 2, Nguyen (Fig. 2) further discloses that the first and the second soldering portions are in the vicinity of and distant from the encapsulant resin, respectively.

Regarding claims 3-4, 10 and 16, Nguyen (Fig. 2) further discloses that each of the first and the second soldering portions is substantially parallel to the interface layer 210, and the interface layer 210 is made of a hard dielectric material of FR-4 (paragraph [0019]).

Regarding claims 6, 12 and 18, Nguyen (Fig. 2) further discloses that the IC chip for each of the first IC package unit $110_{(K+1)}$ and the second IC package unit $110_{(K)}$ is selected from a group consisting of a memory chip (paragraph [0014], lines 15-19).

Regarding claims 7-8 and 13-14, Nguyen (Fig. 2) also discloses that each of the first IC package unit $110_{(K+1)}$ and the second IC package unit $110_{(K)}$ is a thin small outline package (TSOP) or a quad flat pack (QFP) (paragraph [0014], lines 19-24).

3. Claims 5, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (U.S Pub. 2003/0079909) in view of King et al. (U.S Pat. 5,677,566) as applied to claims 1, 9 and 15 above, and further in view of James et al. (U.S Pub. 2003/0201525).

As discussed in details above, the combination of Nguyen and King substantially reads on claims 5, 11 and 17.

Neither Nguyen nor King discloses that the interface layer is made of a soft dielectric material.

However, James (Fig. 1) teaches the forming of a stacked IC comprising semiconductor devices 28 mounted on opposite side of an interposer or support substrate 14 made of a flexible material or a more rigid material (paragraphs [0041] and [0042]). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the interface layer 210 of Nguyen by using a hard dielectric material or a soft dielectric material because as taught by James, such the interface layer materials are commonly used for providing the support for the semiconductor devices (paragraph [0042]) and for providing the wiring connections between the semiconductor devices (see paragraph [0043]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
June 22, 2005.